Ordering number: EN 4037C

Monolithic Linear IC

LA7577N

Super-split PLL-II VIF and SIF IF Signal Processor for TV/VTRs

Overview

The LA7577N is a high tone quality and high picture quality, video IF and sound IF IC. It employs split processing of the video IF signal and sound IF signal using SAW filters and a PLL detector. Further, the PLL detector incorporates a buzz canceler for Nyquist buzz interference suppression to achieve high tone quality.

Functions

VIF stage

- VIF amplifier
- PLL detector
- B/W noise canceler
- RF AGC
- VCO
- Equalizer amplifier
- AFT
- APC detector
- APC filter
- Lock detector
- IF AGC
- Buzz canceler

1st SIF stage

- Preamplifier with AGC
- 1st SIF detector

SIF stage

- SIF limiter amplifier
- FM quadrature detector

Mute stage

- Sound mute (pin 2)
- AV mute (pin 4)
- IS-15 switch (pin 13)

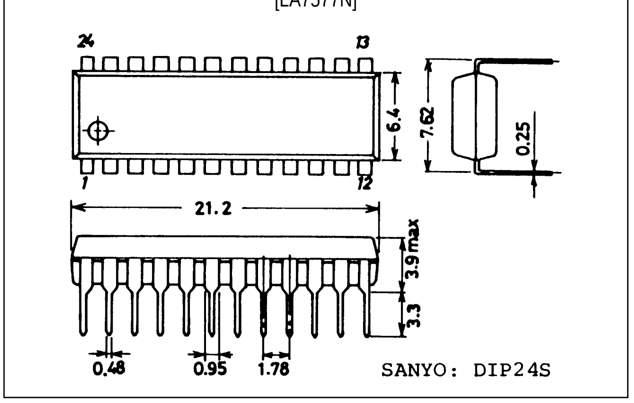
Features

- Employs split processing for wide bandwidth video characteristics
- PLL detector with buzz canceler for excellent buzz and buzz beat characteristics
- APC time constant switch built-in
- High-speed AGC supports double time constant method
- SIF carrier level AGC in the 1st SIF stage for good SIF weak electric field characteristics
- Good differential gain and phase characteristics
- RF AGC easily adjusted using a variable resistor

Package Dimensions

unit: mm

3067-DIP24S



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		13.8	V
Allowable power dissipation	Pd max	Ta ≤ 50°C	1200	mW
Circuit voltages	V_3, V_{13}		V_{CC}	V
	V_{11}		V_{CC}	V
	V_{23}		V_{CC}	V

Parameter	Symbol	Conditions	Ratings	Unit
Circuit currents[1]	I_1		–1	mA
	I_{17}		–10	mA
	I_{21}		–3	mA
	I_{22}		–2	mA
	I_{10}		3	mA
Operating temperature range	Topg	V_{CC} = 9V, Ta = –20 to +75°C	–20 to +70	°C
Storage temperature range	Tstg		–55 to +150	°C

1. Current flowing into the IC is positive and current flowing out is negative.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{CC}	9 or 12	V
Operating supply voltage range	V_{CC} op	8.2 to 13.2	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

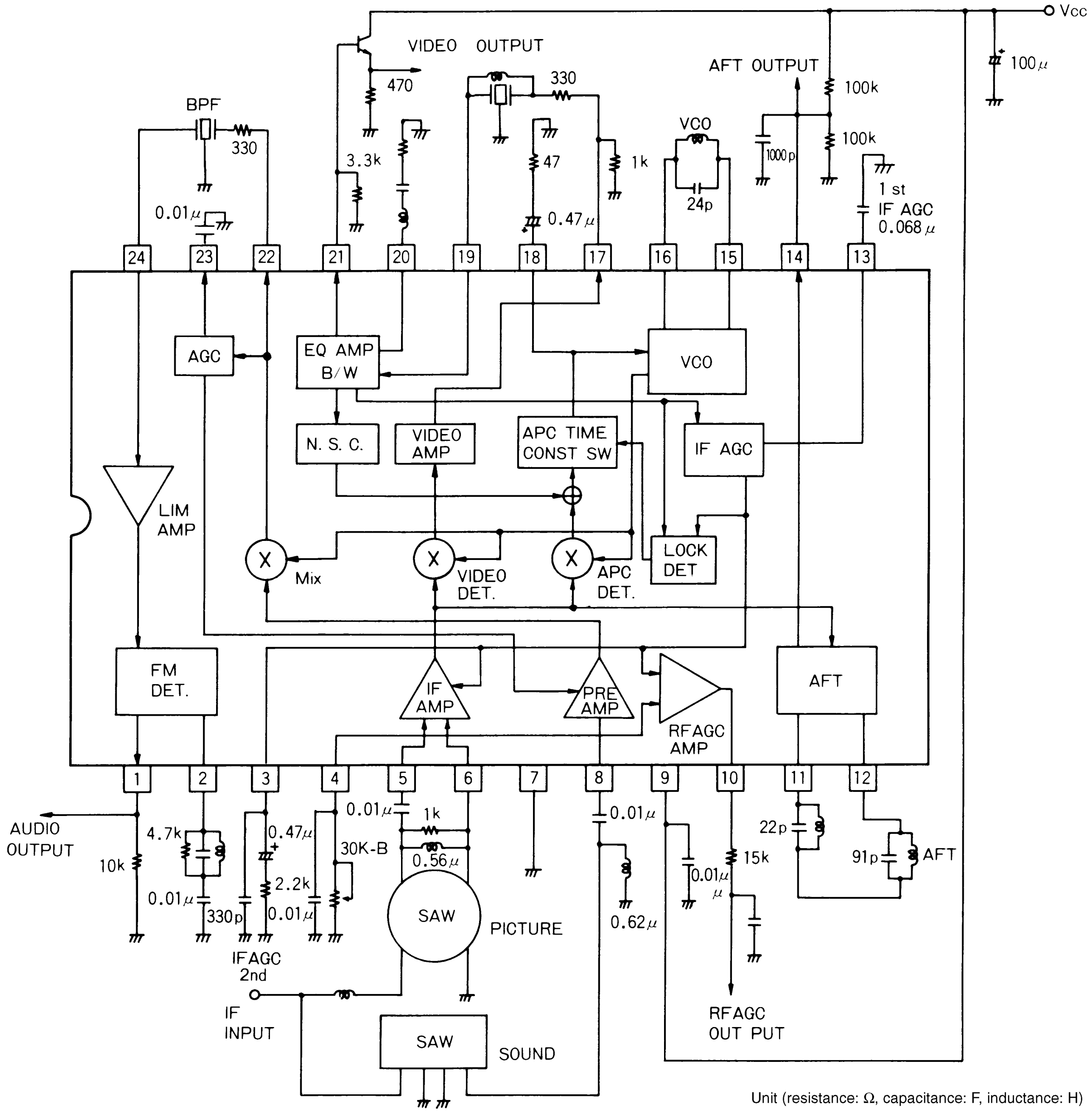
Parameter	Symbol	Conditions	min	typ	max	Unit
[VIF]						
Circuit current	I_9	V_{13} = 5V	44	55	68	mA
Quiescent video output voltage	V_{21}	V_{13} = 5V	6.6	7	7.4	V
Maximum RF AGC voltage	V_{10H}	V_{13} = 7V	10.6	11	11.4	V
Minimum RF AGC voltage	V_{10L}	V_{13} = 7V	–	0	0.5	V
Quiescent AFT voltage	V_{14}	V_{13} = 5V	3.0	5.9	8.0	V
Input sensitivity	V_i		33	39	45	dB/µV
AGC dynamic range	GR		59	65	–	dB
Maximum allowable input	V_i max		100	105	–	dB/µV
Video output amplitude	V_o (video)		1.95	2.25	2.55	Vp-p
Output signal-to-noise ratio	S/N		49	55	–	dB
Sync signal tip voltage	V_{21} (tip)	V_i = 10mV	4.15	4.45	4.75	V
920kHz beat level	I_{920}	P = 0, C = –4dB, S = –14dB	37	43	–	dB
Frequency characteristic	f_C	P = 0, S = –14dB	6	8	–	MHz
Differential gain	DG	V_i = 10mV, 87.5% mod, f_P = 58.75MHz	–	3	6	%
Differential phase	DP		–	2	5	deg
Maximum AFT voltage	V_{14H}		11	11.5	12	V
Minimum AFT voltage	V_{14L}		0	0.4	1.0	V
White-noise threshold voltage	V_{WTH}		8.9	9.3	9.7	V
White-noise clamp voltage	V_{WCL}		5.3	5.7	6.1	V
Black-noise threshold voltage	V_{BTH}		3.4	3.7	4.0	V
Black-noise clamp voltage	V_{BCL}		5.3	5.7	6.1	V
AFT detector sensitivity	S_f		44	60	84	mV/kHz
VIF-stage input resistance	R_i (VIF)	f = 58.75MHz	0.8	1.3	1.75	kΩ
VIF-stage input capacitance	C_i (VIF)	f = 58.75MHz	–	3.0	6.0	pF
APC pull-in range (U)	f_{PU-2}		0.6	1.6	–	MHz
APC pull-in range (L)	f_{PL-2}		–	–1.6	–0.8	MHz
VCO maximum variation range	Δf_U	V_{18} = 3V	0.6	1.6	–	MHz
	Δf_L	V_{18} = 7V	–	–1.6	–0.8	MHz

Parameter	Symbol	Conditions	min	typ	max	Unit
VCO control sensitivity	β	V_{18} = 4.6 to 5V	1.5	3.1	6.2	kHz/mV
[1st SIF]						
4.5MHz conversion gain	VG		21	26	31	dB
4.5MHz output level	V_{SIF1}	V_i = 10mVrms	50	75	110	mVrms
1st SIF stage maximum input	V_{SIF} max	+2.2dB, –1dB	60	70	-	mVrms
1st SIF stage input resistance	R_i (SIF1)	f = 54.25MHz	1.2	2	2.7	kΩ
1st SIF stage input capacitance	C_i (SIF1)	f = 54.25MHz	–	3	6	pF
[SIF]						
SIF limiting sensitivity	V_i (lim)	V_{13} = 5V	–	33	39	dB/µV
FM detector output voltage	V_o	V_{13} = 5V	400	600	790	mVrms
AM rejection	AMR	V_{13} = 5V	40	49	–	dB
Total harmonic distortion	THD	V_{13} = 5V	–	0.5	1.0	%
SIF signal-to-noise ratio	S/N (SIF)	V_{13} = 5V	60	78	–	dB
[Mute, Defeat]						
AFT defeat start voltage	V_{D11}		0.5	2.3	–	V
AV mute threshold	V_{4TH}		0.5	1.9	–	V
FM mute threshold	V_{2TH}		0.5	2.0	–	V
AFT defeat voltage	V_{D14}		5.4	6	6.6	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 9V

Parameter	Symbol	Conditions	min	typ	max	Unit
[VIF]						
Circuit current	I_9	V_{13} = 5V	39	48	59	mA
Quiescent video output voltage	V_{21}	V_{13} = 5V	5.0	5.4	5.8	V
Maximum RF AGC voltage	V_{10H}	V_{13} = 7V	7.6	8	8.4	V
Minimum RF AGC voltage	V_{10L}	V_{13} = 7V	–	0	0.5	V
Quiescent AFT voltage	V_{14}	V_{13} = 5V	2.6	4.5	6.0	V
Input sensitivity	V_i		37	43	49	dB/µV
Video output amplitude	V_o (video)		1.5	1.75	2.0	Vp-p
Sync signal tip voltage	V_{21} (tip)	V_i = 10mV	3.25	3.55	3.85	V
Maximum AFT voltage	V_{14H}		8	8.5	9.0	V
Minimum AFT voltage	V_{14L}		–	0.3	1.0	V
White-noise threshold voltage	V_{WTH}		6.8	7.2	7.6	V
White-noise clamp voltage	V_{WCL}		4.0	4.4	4.8	V
Black-noise threshold voltage	V_{BTH}		2.5	2.8	3.1	V
Black-noise clamp voltage	V_{BCL}		2.5	4.1	4.5	V
AFT detector sensitivity	S_f		28	39	55	mV/kHz
[SIF]						
FM detector output voltage	V_o	V_{13} = 5V	400	600	790	mVrms
[Mute, Defeat]						
AFT defeat start voltage	V_{D11}		0.5	1.6	–	V
AV mute threshold	V_{4TH}		0.5	1.1	–	V
FM mute threshold	V_{2TH}		0.5	1.9	–	V
AFT defeat voltage	V_{D14}		3.9	4.5	5.1	V

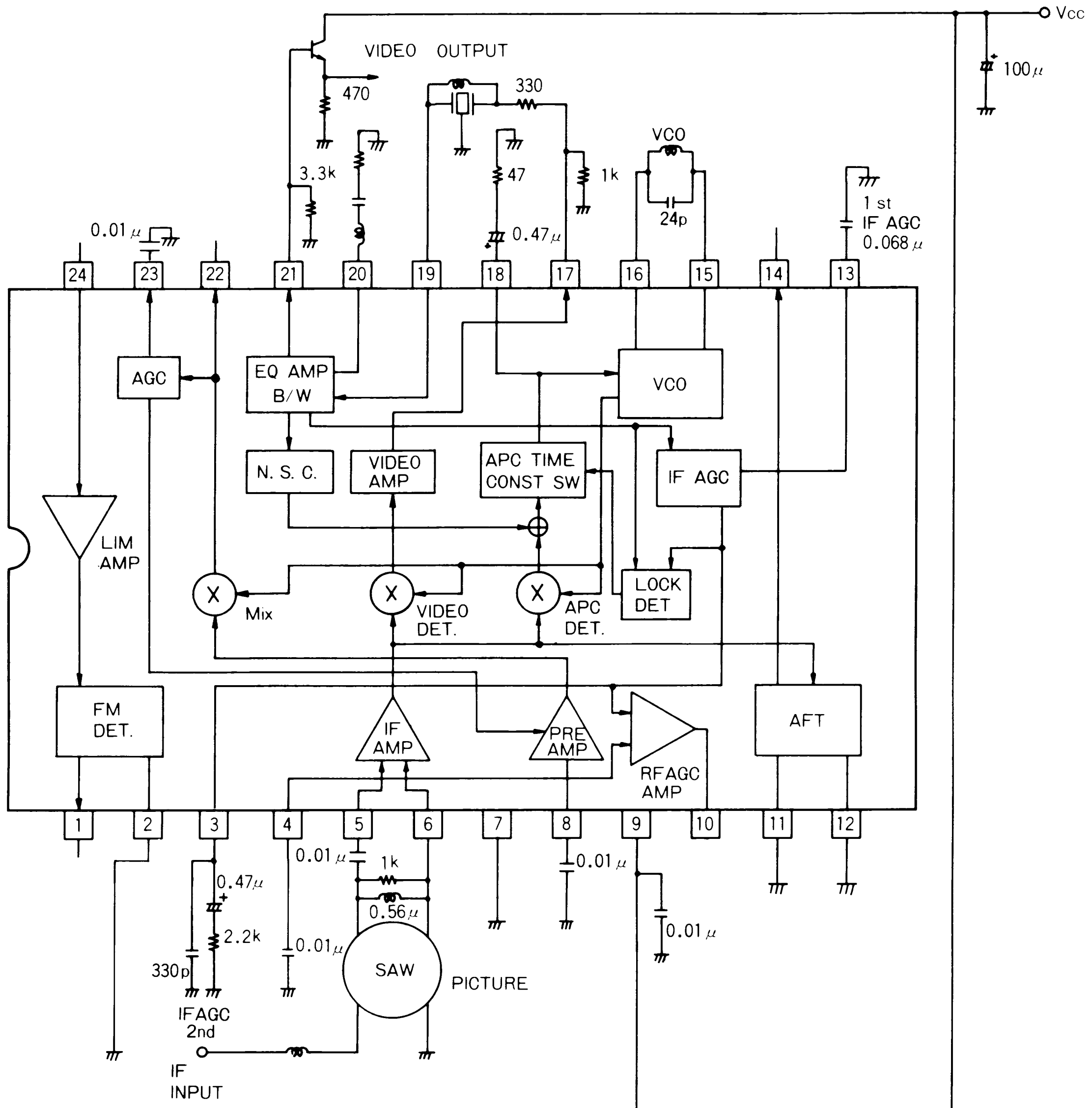
Sample Application Circuit (Japan)



Unit (resistance: Ω, capacitance: F, inductance: H)

Sample Application Circuit (Japan)

(when the SIF, 1st SIF, AFT and RF AGC are not used)



Unit (resistance: Ω, capacitance: F, inductance: H)

When the SIF stage is not used

- Leave pin 1 open
- Tie pin 2 to GND
- Leave pin 24 open

When the 1st SIF stage is not used

- Connect a 0.01μF capacitor between pin 8 and GND (leave the 0.01μF capacitor on pin 23 connected to GND)
- Leave pin 22 open

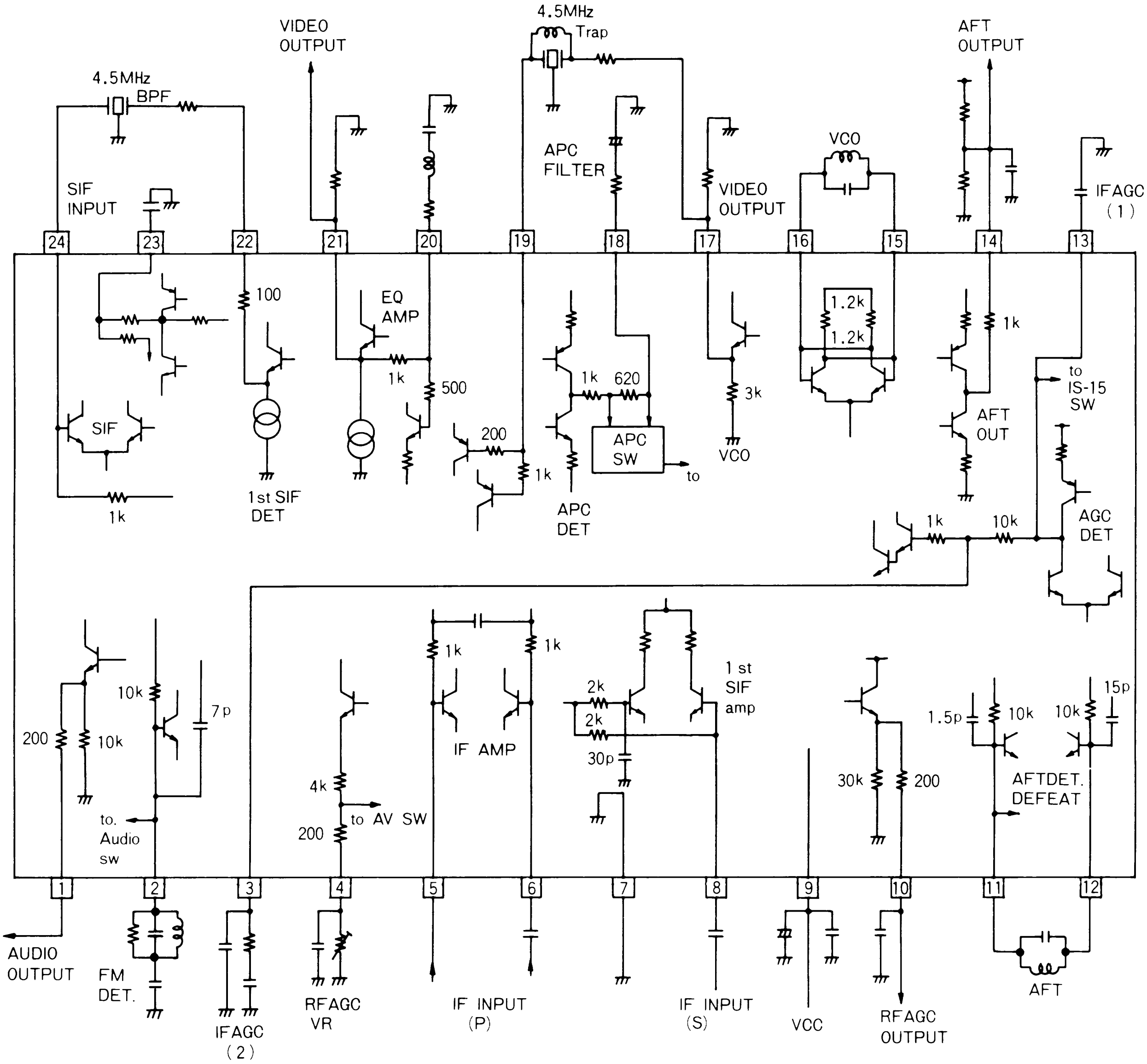
When the AFT circuit is not used

- Tie pins 11 and 12 to GND
- Leave pin 14 open

When the RF AGC circuit is not used

- Connect a 0.01μF capacitor between pin 4 and GND
- Leave pin 10 open

LA7577N Interface Circuit



Buzz Canceler

Phase-locked loop (PLL) detectors feature lower harmonic distortion in the video stage, higher IF phase differential suppression and much lower audio buzz than conventional quasi-synchronous detectors. However, voltage-controlled oscillators (VCO) in PLL detectors, generally, are highly susceptible to interference from flyback pulses. This interference can affect the frequency of the VCO, resulting in added output noise components and audio buzz. This interference is minimized by VCO supply voltage regulation.

The PLL detector is shown in Figure 1. The automatic phase control (APC) circuit multiplies the IF signal by the VCO output signal, which is phase shifted by 90°, to suppress the AM component. The APC output is passed through a low-pass filter to form the VCO control signal. This results in a signal with a good carrier-to-noise ratio (C/N).

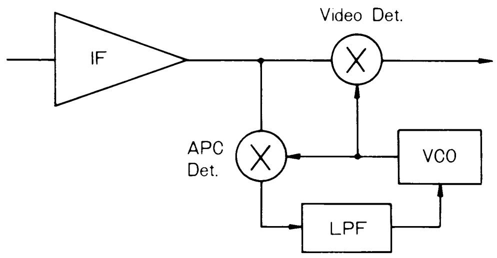


Figure 1. PLL detector

A simple PLL detector, however, can cause other audio problems, because the broadcast signal is transmitted using vestigial sideband modulation. In this case, the RF signal is converted to an IF signal by the Nyquist slope of the SAW filter. Since the sidebands in the vicinity of the picture carrier are attenuated, the magnitudes of the upper and lower sideband vectors are different. The result is a phase distortion component, θ,in the composite vector as shown in Figure 2.

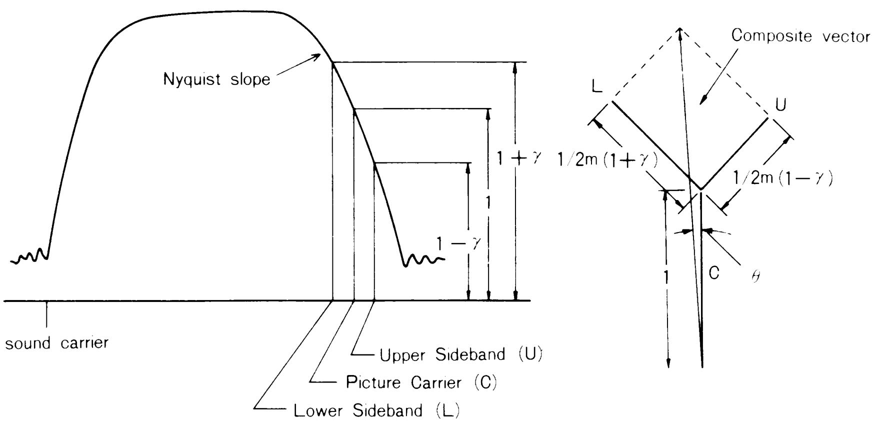


Figure 2. Phase noise component

This phase distortion is the cause of audio buzz, or Nyquist buzz, because the VCO synchronizes to the composite vector. A Nyquist buzz cancelation circuit is incorporated into the LA7577N to reduce the level of this noise as shown in Figure 3.

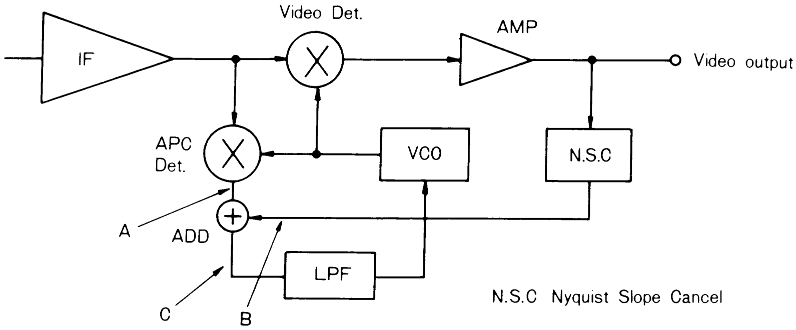


Figure 3. PLL detector with buzz cancelation

A typical signal with Nyquist buzz is shown in Figure 4 together with the compensating signal generated by the Nyquist-slope canceler and the resultant signal.

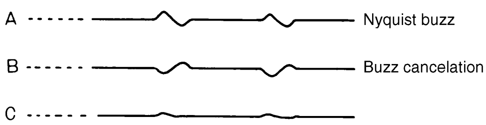


Figure 4. Nyquist buzz cancelation waveforms

The circuit shown in Figure 3 is highly effective in suppressing audio buzz caused by the 4.5MHz IF beat signal in Japanese multiplexed (L – R) audio or American (MTS) Multichannel TV Sound (L – R) signals.

As buzz cancelation is independent of the PLL loop time constant, other parameters such as automatic phase control can be optimized to eliminate interference from flyback pulses.

Design Notes

FM Detector Output (Pin 1)

The FM detector output is an emitter follower with a 200Ω series protection resistor as shown in Figure 5.

In multiplex audio applications where pin 1 is connected to the input of a multiplexed audio decoder, the input resistance of the decoder can decrease, causing distortion of the (L − R) signal. In this case, a 5.1kΩ or larger resistor, R1, should be connected between pin 1 and ground.

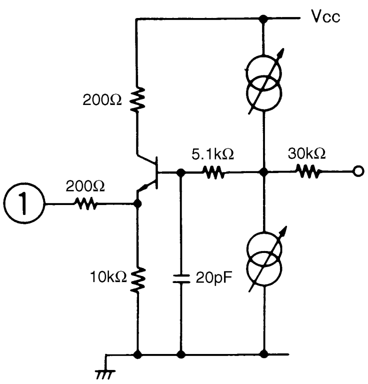


Figure 5. FM detector output

In monophonic applications, an RC de-emphasis circuit should be connected as shown in Figure 6. The time constant is given by R2 × C.

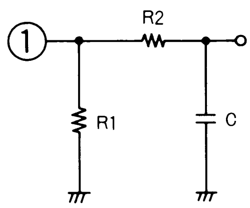


Figure 6. RC de-emphasis circuit

FM Discriminator (Pin 2)

The quadrature detector frequency at which the 90° phase shift occurs is determined by the tuned circuit connected to pin 2 as shown in Figure 7.

The detector bandwidth characteristics are determined largely by the coil Q and damping resistance. The damping resistor should be chosen for the desired output level and bandwidth characteristics.

FM muting is achieved by holding point A, in Figure 7, at ≤1V DC.

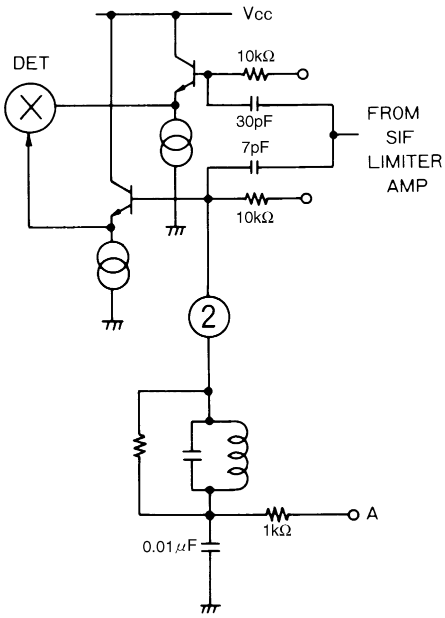


Figure 7. FM discriminator

IF AGC (Pins 3 and 13)

The IF signal is peak detected and averaged by the filters connected to pins 13 and 3, which are the 1st AGC and 2nd AGC, respectively, as shown in Figure 8. The IF AGC audio component of the input signal to the video IF stage is first removed by an audio trap.

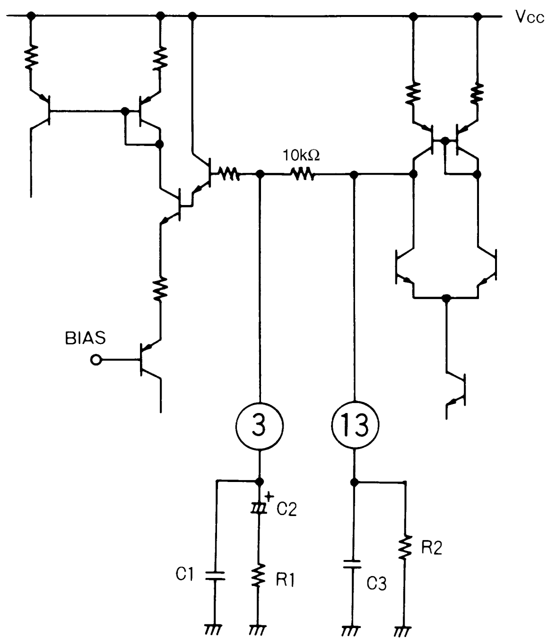


Figure 8. IF AGC circuits

Typical AGC filter time constants

Pin	Component	Single time constant	Double time constant	
3	C1	330pF	330pF	330pF
	R1	–	2.2kΩ	1.8kΩ
	C2	–	0.47μF	0.1μF
13	C3	0.47μF	0.068μF	0.047μF
	R2	820kΩ	820kΩ	820kΩ

Mute switch (IS-15 switch)

The black-noise canceler can be disabled by pulling pin 13 to 1V or lower. An external AGC source can then be applied to pin 3 to drive the AGC circuit. This mode of operation is designed for use with an IS-15 (EIA standard) switch.

Ghosting problems

Reflected signals which have a phase different from that of the main signal can cause distortion of the horizontal sync pulse, as shown in Figure 9. As a result, the same charge-to-discharge current ratio of the IF AGC cannot be maintained. If the phase difference is large, the video signal can also be distorted as shown in Figure 10. Distortion can be minimized by connecting a 820kΩ to 1MΩ resistor between pin 13 and ground.

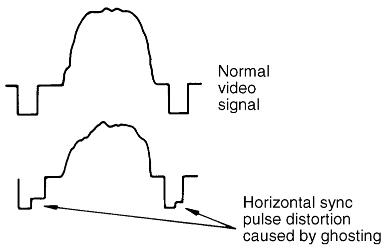


Figure 9. Horizontal sync pulse distortion

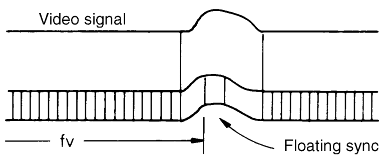


Figure 10. Video signal distortion

RF AGC Variable Resistor (Pin 4)

The operating point of the RF AGC can be adjusted using a variable resistor connected to pin 4 as shown in Figure 11. When pin 4 is pulled to 0.5V or lower, both the FM and video outputs are muted.

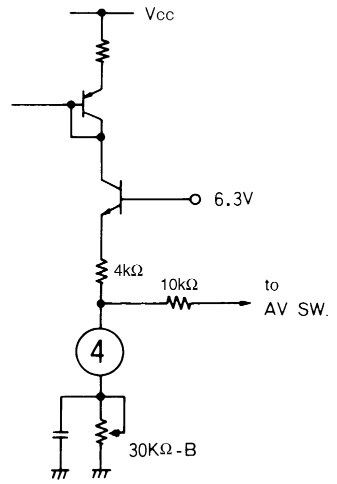


Figure 11. RF AGC adjustment

VIF Input (Pins 5 and 6)

The VIF amplifier inputs on pins 5 and 6 should be capacitively coupled to block DC. The input signal is the average of the signals on these inputs. The input resistance is approximately 1.5kΩ and the input capacitance is approximately 3pF.

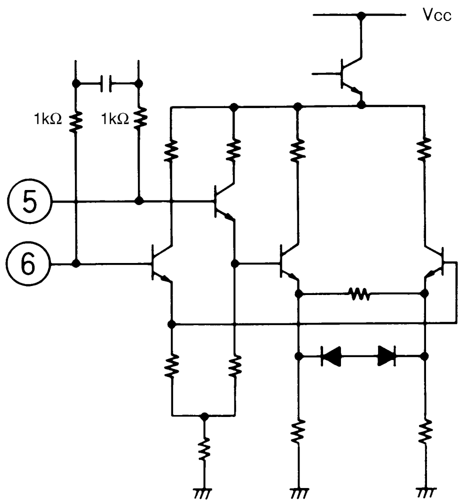


Figure 12. VIF stage

1st SIF Input (Pin 8)

The 1st SIF amplifier input on pin 8, shown in Figure 13, should be capacitively coupled to block DC. If a SAW filter is used, an inductor should also be connected as shown in Figure 14. This matches the SAW filter output capacitance to the LA7577N input capacitance and increases the sensitivity. The inductor typically would be 0.62μH (for Japan), 1.0μH (for the USA) or 1.3μH (for PAL countries).

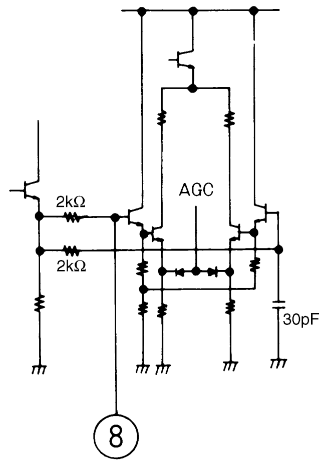


Figure 13. 1st SIF stage

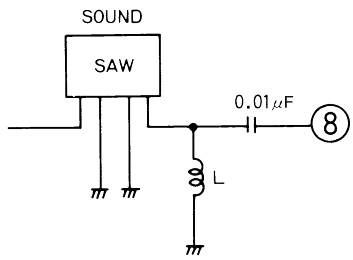


Figure 14. SAW filter matching

RF AGC Output (Pin 10)

The RF AGC output on pin 10 is an emitter follower with a 200Ω series protection resistor as shown in Figure 15. The value of the bleeder resistor connected between pin 10 and the tuner, shown in Figure 16, should be chosen based on the tuner maximum gain.

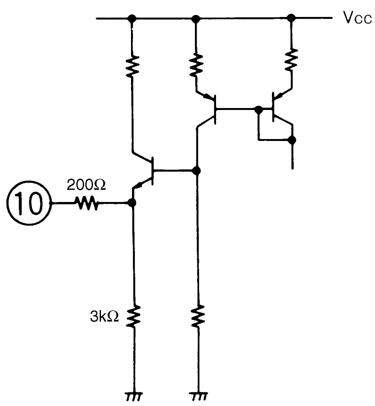


Figure 15. RF AGC output

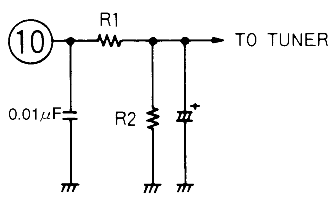


Figure 16. Bleeder resistor connection

AFT Tank (Pins 11 and 12)

The automatic frequency tuner (AFT) tank connected to pins 11 and 12 generates the 90° phase shift required for quadrature detection. The band-pass frequency characteristics of the IF SAW filter and the AFT tank are shown in Figure 17(A) and 17(B), respectively. The combined response is shown in Figure 17(C). The resulting extended low-frequency response, which increases susceptibility to incorrect operation, can be reduced by connecting capacitor C2 in series with the AFT tank as shown in Figure 18. The resultant frequency response is shown in Figure 17(D).

Capacitors C1 and C2 should have a ratio of approximately 5 to 1. An inductor or resistor should also be connected in parallel with C2 to maintain the DC balance of the AFT tank.

The AFT can be defeated by connecting pin 11 to ground through resistor R1, which should be 20kΩ or lower.

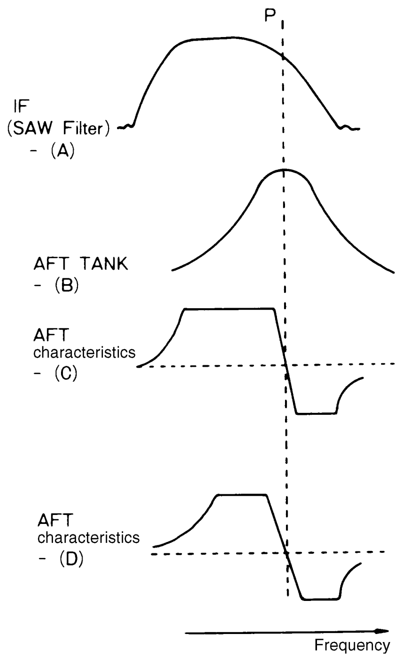


Figure 17. AFT tank characteristics

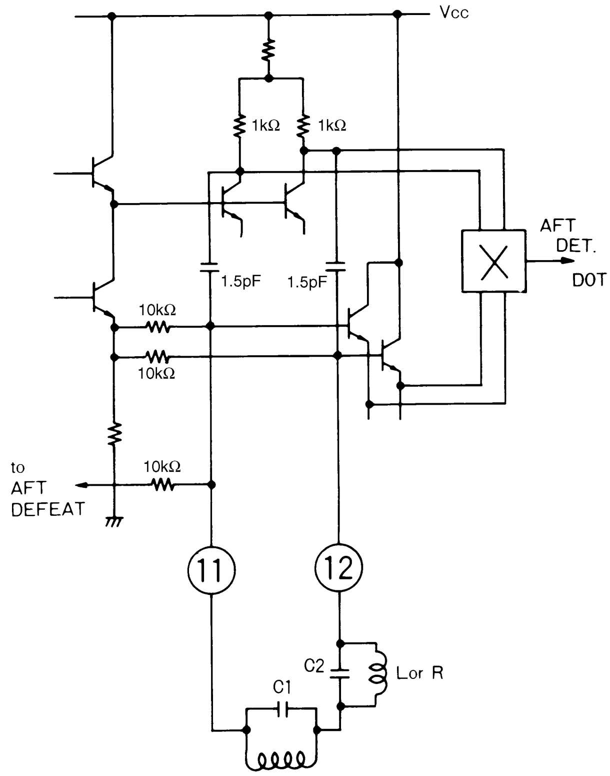


Figure 18. AFT tank

AFT Output (Pin 14)

An external bleeder resistor is required to generate the AFT voltage. The AFT loop time constant is formed by external resistor R3 and capacitor C2, as shown in Figure 19. The resistor also provides overvoltage protection.

Fluctuations in the AFT quiescent output voltage, if present in station selector systems using PLLs or voltage synthesizers, can be reduced by connecting series resistor R4 as shown in Figure 20. Note, however, that this also reduces the AFT range.

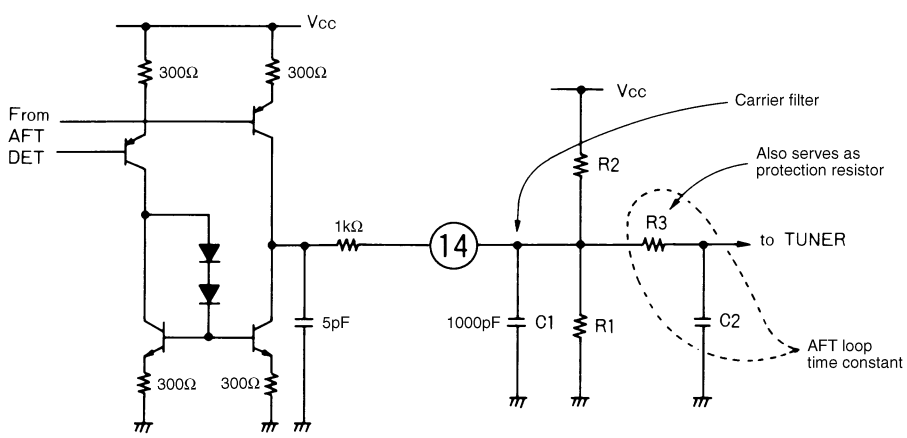


Figure 19. AFT loop time constant

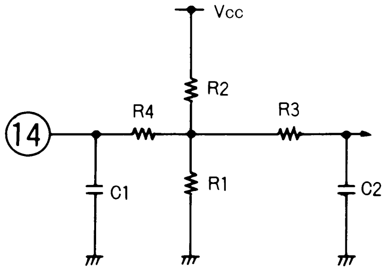


Figure 20. AFT output

VCO Tank (Pins 15 and 16)

The VCO tank circuit is shown in Figure 21. The tank circuit capacitors connected between pins 15 and 16 should be in the range 20 to 27pF (24pF is recommended). The VCO tank susceptibility to external effects can be reduced by using either chip capacitors or capacitors integrated with the tank coil.

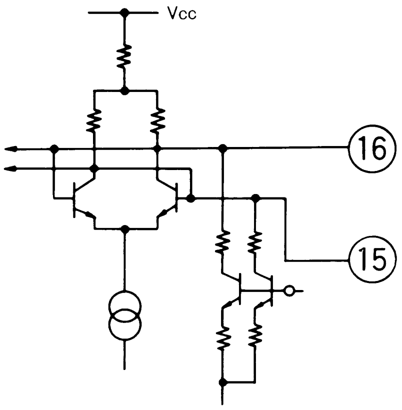


Figure 21. VCO tank

Composite Video Output (Pin 17)

The 4.5MHz composite video output circuit is shown in Figure 22. A resistor should be connected between this emitter-follower output and ground to ensure adequate output drive capability. The resistor should be ≥1.2kΩ (V_{CC} = 12V), or ≥1kΩ (V_{CC} = 9V).

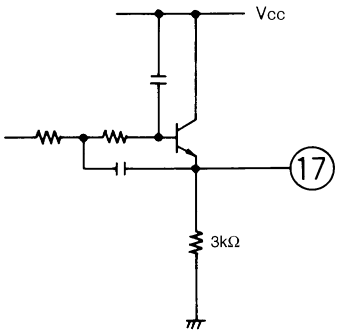


Figure 22. Composite video output

APC Filter (Pin 18)

Time-constant switching is incorporated into the VCO for automatic phase control (APC). When the PLL is locked, the VCO is controlled by loop A, shown in Figure 23. When the PLL is unlocked or the signal is weak, the VCO is controlled by loop B which has higher gain. The increased APC loop gain also increases the pull-in range. The recommended range for the external APC filter resistor is 47 to 150Ω, and for the capacitor, 0.47μF.

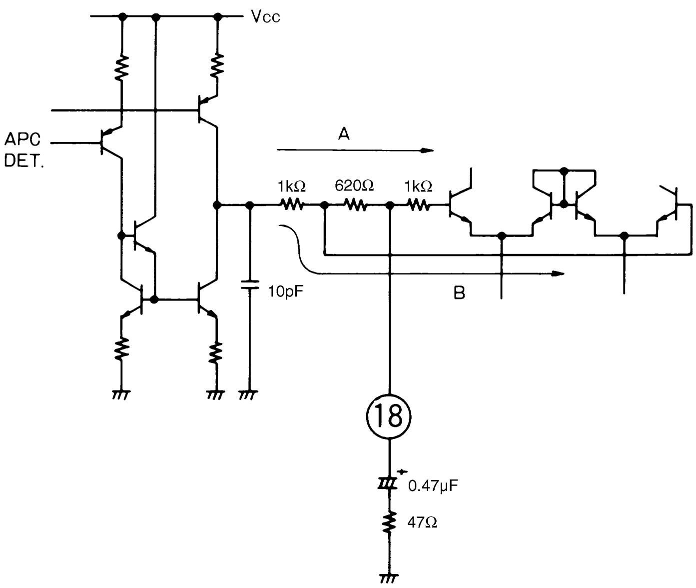


Figure 23. APC filter

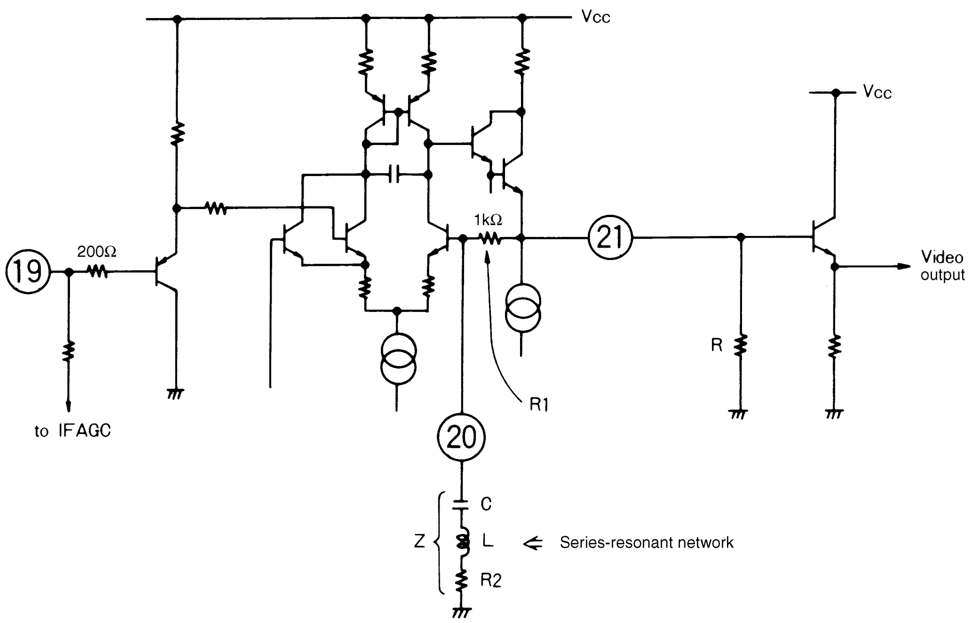


Figure 24. Equalization amplifier

Equalization Amplifier (Pins 19 to 21)

The video signal, after passing through the 4.5MHz trap, is input on pin 19 to the equalization amplifier, and output on pin 21. A resistor should be connected between the emitter-follower output and ground to ensure adequate output drive capability. The resistor should be ≥2.7kΩ (V_{CC} = 12V) or ≥2.2kΩ (V_{CC} = 9V). A buffer transistor should be used if the signal is taken off-board.

Equalization amplifier design

The equalization amplifier has an external series resonant circuit, shown in Figure 24, which controls the frequency characteristic. The output voltage, V_o, is given by the following equation:

$$V_o = (R1/Z + 1)\,(V_i + V_{in})$$

Since the input voltage, V_{in}, is small, the gain is given approximately by the following equation:

$$A_V = V_o/V_i = R1/Z + 1$$

The amplifier can be used as a voltage amplifier by connecting a network to pin 20 as shown in Figure 25. The bleeder resistor should be chosen to avoid excessive gain and extreme video sync tip voltages.

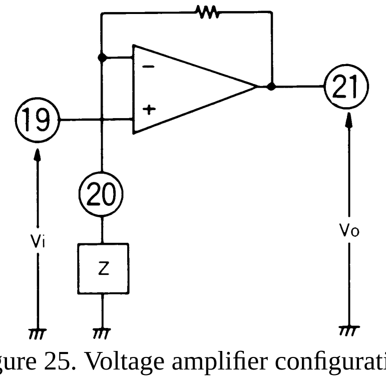


Figure 25. Voltage amplifier configuration

External bleeder resistor selection

If the equalization amplifier is configured for non-unity gain, bleeder resistors R2 and R3, shown in Figure 26, are required to ensure that the output DC voltage does not change.

The sync tip voltage does not change if V_X is approximately equal to V_{21}. V_X is given by the following equation:

$$V_X = V_{CC} \times R2/(R2 + R3)$$

The voltage gain is given by:

$$A_V = 1 + 1000/Z1$$

where

$$Z1 = R2 \times R3/(R2 + R3)$$

and resistors R2 and R3 are given by:

$$R2 = 1000 \times V_{CC}/[(V_{CC} - V_X) \times (A_V - 1)]$$
$$R3 = 1000 \times V_{CC}/[V_X \times (A_V - 1)]$$

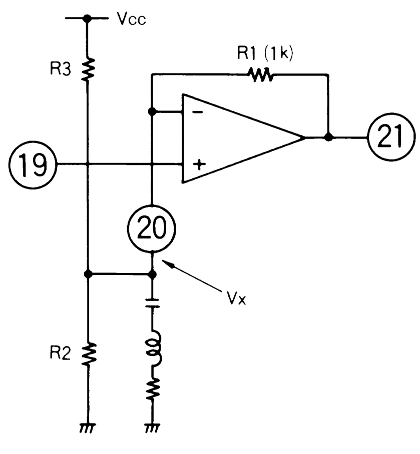


Figure 26. External bleeder resistor circuit

1st SIF Output (Pin 22)

The 1st SIF output is an emitter follower with internal 100Ω series resistor as shown in Figure 27. An additional series resistor should be used for impedance matching to the ceramic band-pass filter.

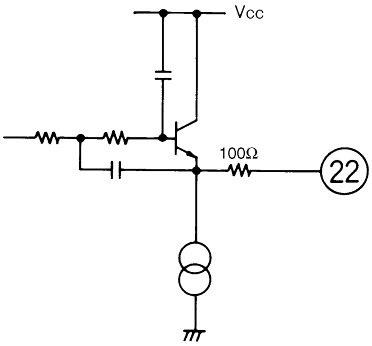


Figure 27. 1st SIF output

1st SIF AGC Filter (Pin 23)

The 1st SIF amplifier has an AGC range of approximately 30dB. The capacitor on pin 23 is normally 0.01µF, but may, depending on the situation, be as large as 4.7µF (4.7µF is recommended when using the filter for NICAM signal processing).

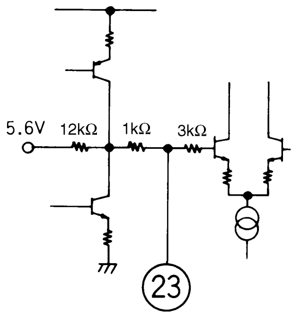


Figure 28. 1st SIF AGC filter

SIF Input (Pin 24)

The input impedance of the amplifier, shown in Figure 29, is approximately 1kΩ. Any interference on pin 24, a video signal for example, can cause audio buzz or heterodyning. Good circuit board layout is essential. Examples of both good and poor layout are shown in Figure 30.

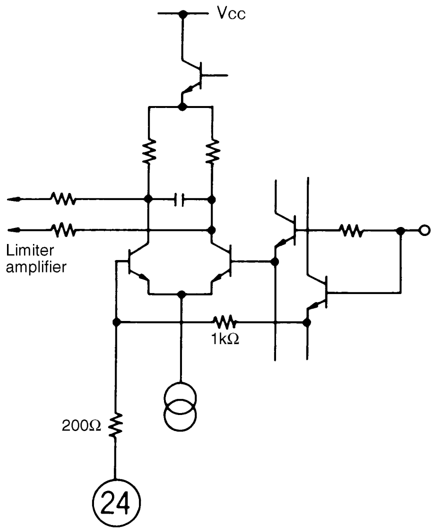


Figure 29. SIF stage input circuit

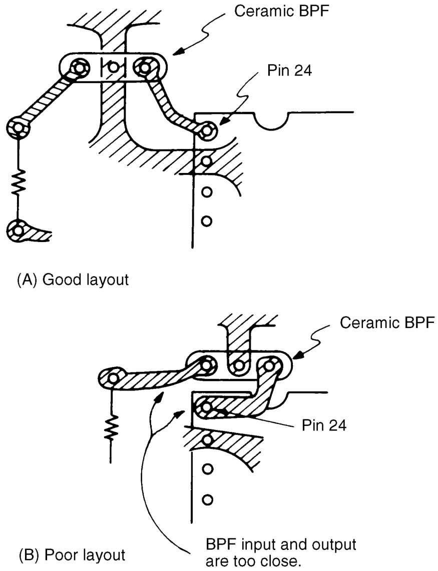


Figure 30. PCB layout examples

Sanyo SAW Filters

Two types of surface acoustic wave (SAW) filter built on different piezoelectric substrates can be used with the LA7577N—Lithium Tantalate and Lithium Niobate.

Lithium Tantalate ($LiTaO_3$) SAW filters

$LiTaO_3$ SAW filters have a low temperature coefficient of −18ppm/°C and good stability, but have high insertion loss. An external coil is required at the output for level matching as shown in Figure 31.

$LiTaO_3$ SAW filters cover the Japanese and American bands, which both have relatively high IF frequencies. These filters have part numbers of the form TSF1××× or TSF2×××.

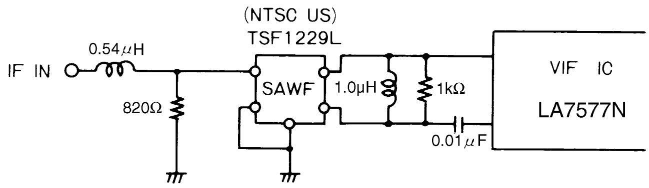


Figure 31. $LiTaO_3$ SAW filter

Lithium Niobate ($LiNbO_3$) SAW filters

$LiNbO_3$ SAW filters have a relatively high temperature coefficient of −72ppm/°C, but have an insertion loss approximately 10dB lower than $LiTaO_3$ filters. A matching circuit is, therefore, not required at the output, as shown in Figure 32. As a result of the lower insertion loss, the pass-band ripple is higher. However, the low impedance and low feedthrough of these filters make them less susceptible to stray capacitance effects caused by external components and PCB layout, resulting in greater stability.

$LiNbO_3$ SAW filters cover the PAL and American bands, which have relatively lower IF frequencies. These filters have part numbers of the form TSF5×××.

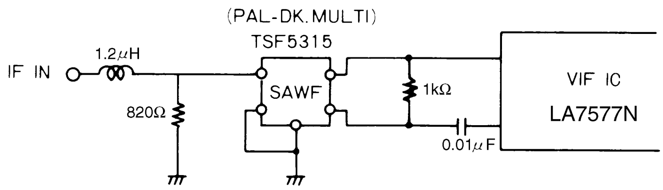


Figure 32. $LiNbO_3$ SAW filter

VCO Tank Circuit

VCO tank circuit with built-in capacitor

When the IC power supply is switched ON, the heat generated by the IC is conducted by the PCB, including into the VCO tank. The tank coil legs effectively act as a heatsink and the heat is dissipated, such that an insignificant amount of heat is conducted into the VCO tank capacitor. As a result, the effect on VCO drift is made smaller.

Even so, it is recommended that the inductor and capacitor be chosen so that their temperature characteristics effectively cancel. Accordingly, it is preferable to use inductors with low temperature coefficient cores and low temperature coefficient capacitors.

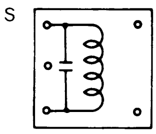
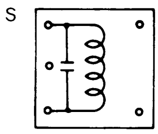
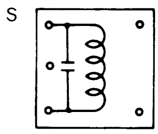
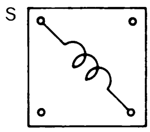
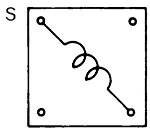
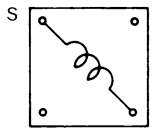
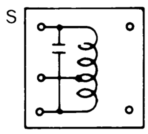
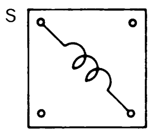
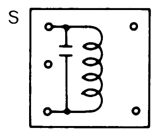
VCO tank circuit with external capacitor

If using an external capacitor, the heat generated by the IC is conducted by the PCB, including to the external capacitor. If this happens, the heat affects the capacitor and changes its capacitance value.

However, because the VCO tank coil is not significantly affected, the VCO tank tuning point changes.

In this case, it is highly preferable to use inductors with low temperature coefficient cores and low temperature coefficient capacitors.

Coil Specifications

Component	Japan f = 58.75MHz	USA f = 45.75MHz	PAL countries f = 38.9MHz
VCO coil T_1	 6T 0.12ϕ C = 24pF HW6226-4	 9T 0.12ϕ C = 24pF HW6227-4	 11T 0.12ϕ C = 24pF MA6389
AFT coil T_2	 3.5T 0.5ϕ MA8181	 5.5T 0.5ϕ MA6343	 7.5T 0.5ϕ MA7115
SIF coil T_4	 19T 0.08ϕ C = 100pF KS6102-1	 19T 0.08ϕ C = 100pF KS6102-1	 25T 0.08ϕ C = 100pF MA8182
VIF SAW filter (Sanyo)	TSF1132L, TSF1137U	TSF1229L, TSF1241U	TSF5315
SIF SAW filter (Sanyo)	TSB1101P	TSB1205P	–